Digital Optical Module
FPGA Design Requirements

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Introduction

The FPGA in the Digital Optical Module electronics is the main active component besides the low power CPU. It holds the logic for trigger, ATWD readout, lookback buffer management, time calibration and communication. The FPGA is connected to the low power CPU of the DOM like a typical peripheral chip using memory mapped registers inside the FPGA to control various functions of the design.

FPGA properties

An Altera 10K50E device is used. This device has an equivalent of 50000 Gates, 2880 logic cells and 10 memory blocks with 512 bytes. The core operating voltage is 2.5V and the IO-cells can be used at either 2.5V or 3.3V. The inputs can be used with 5V signals and the IO-drivers can drive 5V devices if pull-up resistors are used. The chip has an internal clock PLL which allows to double the external clock frequency. Power consumption is a critical parameter for this design. The 10K50E draws a constant idle current (10mA @ 2.5V core voltage) and a current proportional to clock frequency and the number of switching logic cells. A continuously switching logic cell will consume an average 19uA/MHz. In order to keep the total power consumption low, the number of switching logic cells has to be minimized. This is eased by the fact that most parts of the design have to run at full speed only during short periods of time after a trigger event and are mostly idle.

FPGA configuration

The FPGA is an SRAM-type part and has to be configured by the CPU before a user application can access most of the DOM hardware. Configuration is done either via the serial configuration port or the JTAG port. The configuration data stream has a size of about 500kBits.

Design overview

The design can be partitioned into a number of mostly independent sub-designs which are connected by well defined interfaces. An overview of all sub-designs and the data flows is given in diagram 1.

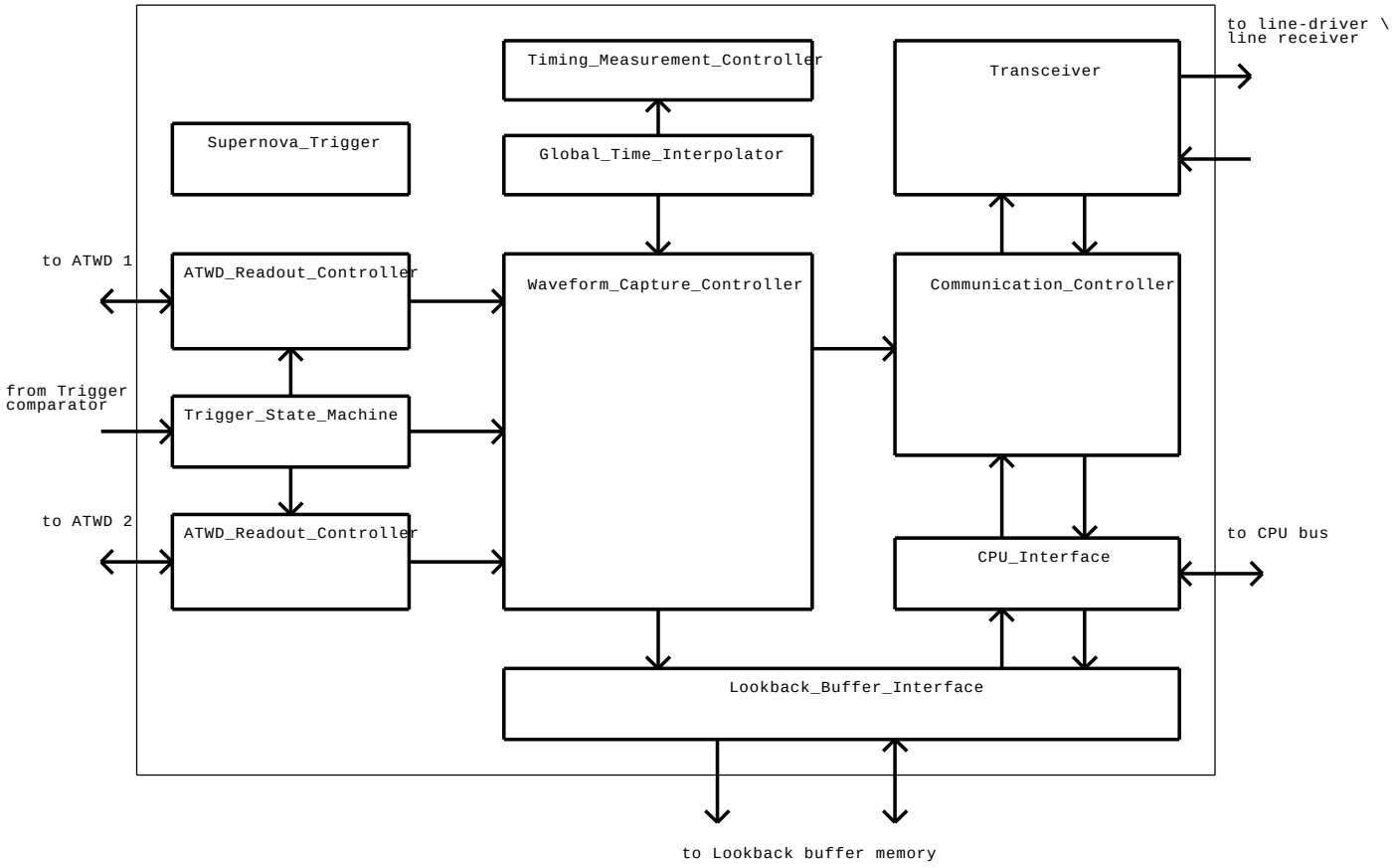

Diagram 1: FPGA sub-designs

CPU-Interface and register set

The FPGA is connected to the CPU using an 8 bit wide data bus and a 23 bit wide address bus. The address map divides the 8 Mbyte address space into three parts:

512 Kbyte pointer table address space addresses 0x400000 to 0x47FFFF),
4 Mbyte waveform table address space (addresses 0x000000 to 0x3FFFFF) and
memory mapped register address space (addresses above 0x7FFF00).

The pointer table and the waveform table together are called the lookback buffer because they are used to store digitized event data needed for the retrival operation initiated by the trigger processor on the surface.

The complete FPGA register set is given in table 1:

Address	Register name	Description
0x400000	Trigger Flag Register– TFReg	Flags to enable/disable trigger signals
0x400001	Readout Control Register– RdContrReg	Readout sequence control
0x400002	Resolution Control Register 0ResContrReg0	Resolution control for Channel 0
0x400003	Resolution Control Register 1ResContrReg0	Resolution control for Channel 1
0x400004	Resolution Control Register 2ResContrReg2	Resolution control for Channel 2
0x400005	Resolution Control Register 3ResContrReg3	Resolution control for Channel 3
0x400006	Ch 0 Digital Threshold Register	Digital Threshold for Channel 0
0x400007	Ch 1 Digital Threshold Register	Digital Threshold for Channel 1
0x400008	Ch 2 Digital Threshold Register	Digital Threshold for Channel 2
0x400009	Ch 3 Digital Threshold Register	Digital Threshold for Channel 3
0x400010	Coarse Time Stamp Counter Byte 0 (LSB)	
0x400011	Coarse Time Stamp Counter Byte 1	
0x400012	Coarse Time Stamp Counter Byte 2	
0x400013	Coarse Time Stamp Counter Byte 3 (MSB)	
0x400014	Current Pointer Register Byte 0 (LSB)	
0x400015	Current Pointer Register Byte 1	
0x400016	Current Pointer Register Byte 2 (MSB)	
0x400017	Slow_ADC_Samples_Register	

Trigger sub-design

The trigger sub-design is responsible for generating the sequence of events initiated by a a trigger signal. This includes determination of trigger event type, ATWD readout, trigger packet generation and waveform storage in the look-back buffer.

The trigger sub-design consists of a state machine with a small number of states. The idle state of the trigger state machine is called *Trigger Idle State*. The system stays in this state until the trigger sequence is started by any one (or any combination) of the following signals:

sPETrigger : The PMT signal is above the single photo electron threshold.
mPETrigger: The PMT signal is above the multiple photo electron threshold.
lLocalCoincidence: A local coincidence signal from the lower DOM was received.
uLocalCoincidence: A local coincidence signal from the upper DOM was received.

Four bits in the Trigger Flag Register(TFReg) are used to enable (1) or disable (0) these input signals in order to select the trigger mode of the system.

Once the trigger sequence is started, any further trigger event is ignored until the trigger system returns to the *Trigger Idle State*.

The first state of the trigger sequence after leaving the idle state is the *Signal Capture State*. The length of this phase is determined by the ATWD sampling speed. The trigger sub-system senses the time needed by the ATWD by waiting for the trigger signal to appear at the Trigger Complete output of the ATWD chip.

The state transitions of the trigger state machine following the Signal Capture state depend on trigger mode bits in the `Readout Control Register` (`RdContrReg`).

The trigger state machine allows to digitize any four ATWD channels once, twice or not at all. The reason for this is that the digitization time is proportional to the number of Digitization Clock counts and the total digitization time has to be kept small in order to have a small dead time. For small signals like the single photoelectron pulses which make up 99% of all events, only ATWD channel 0 has to be digitized with 6-7 bits of resolution.

The resolution for this and the following readout states is set by a three bit wide field in the `Ch x Resolution Control Register` (`ResContrReg`). The meaning of these three bits is given by table 2:

Value	Operation
0	Do not digitize channel at all
1	Digitize with 5 bits precision (i.e. 16 Digitization clock cycles)
2	Digitize with 6 bits precision (i.e. 32 Digitization clock cycles)
3	Digitize with 7 bits precision (i.e. 64 Digitization clock cycles)
4	Digitize with 8 bits precision (i.e. 128 Digitization clock cycles)
5	Digitize with 9 bits precision (i.e. 256 Digitization clock cycles)
6	Digitize with 10 bits precision (i.e. 512 Digitization clock cycles)

Table 2: Resolution Control Register Entries

A simplified version of the resulting state diagram is shown in figure 2. The Chx_Low/High_Enable signals are obtained by ORing all the bits of the Resolution Control Fields for the given channel. The Readout Finished signal is generated by the Waveform Capture Controller whenever digitization and readout of a channel is either finished or prematurely aborted. This is controlled by a fourth bit, the `Skip Ch x Digitization Flag in the Resolution Control Registers`. If any sample exceeds the digitization range given by the `Ch x Digital Threshold Register` and if this flag is 1, the digitization is skipped and the data is not written into the waveform table memory. If this flag is 0, the digitization is carried out independently of any threshold and the data is written into the waveform buffer.

The final trigger state is the Buffer Write state. It is waiting for completion of any lookback buffer write operation of the Waveform Capture Controller.

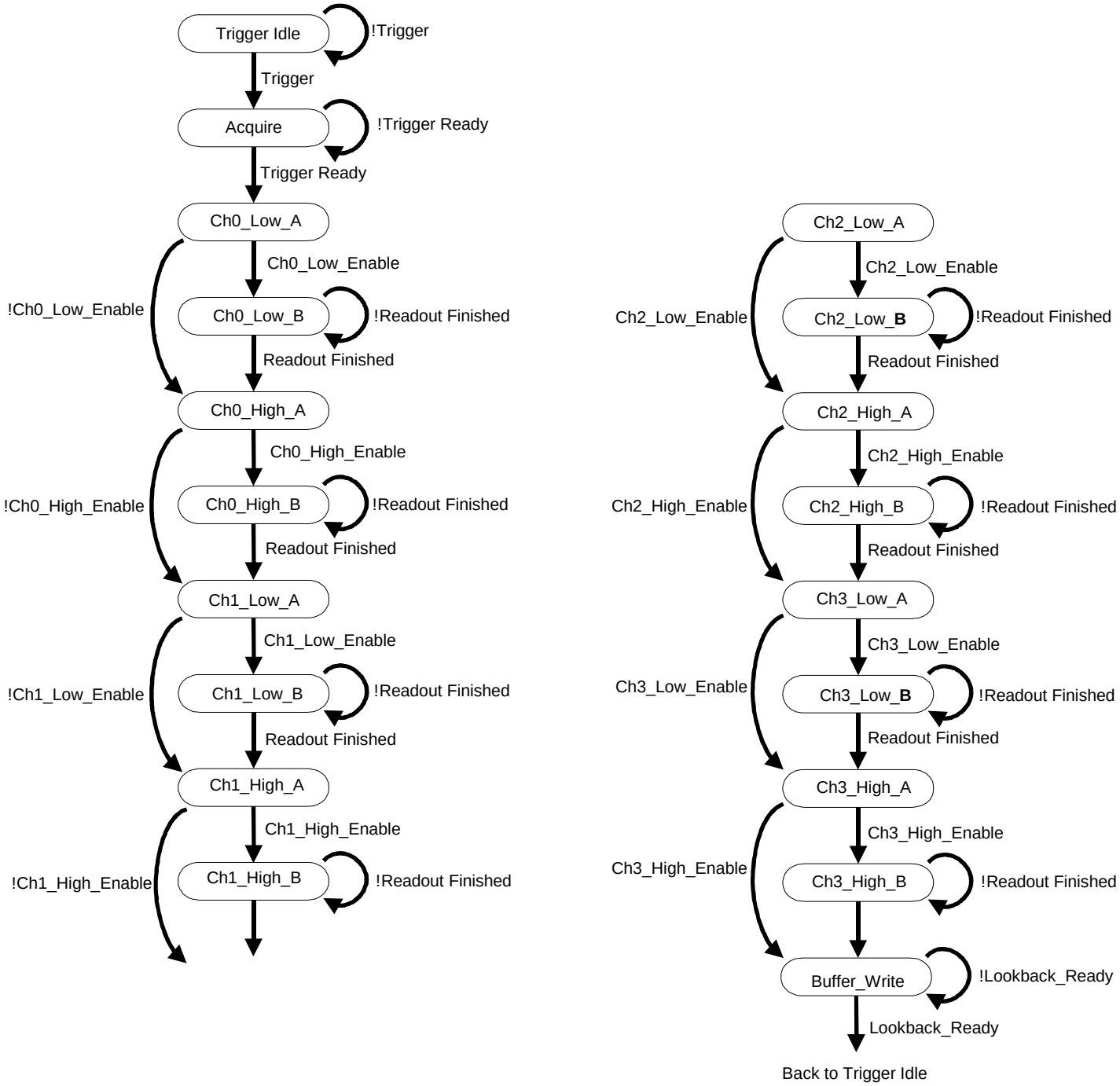

Figure 2: Trigger state machine

ATWD Readout Controller

The generation of the ATWD control signals (except for the `Trigger` signal) is done by the ATWD Readout Controller state machines. The state machine itself is started by a logic 1 applied to the `Start Readout` input and can be stopped at any time by pulling the signal to 0. Once the state machine is started, it performs a digitization of the channel which is given by the value of the `Channel_Select`[1..0] input with a given number of digitization clocks pulses given by the `Resolution_Select[2..0]` input. The state machine is designed in such a way that an abortion of a currently running readout sequence does not lead to a loss of analog waveform information. The state machine generates a `Readout_Controller_Idle` signal to indicate that it has safely finished a readout sequence.

Waveform Capture Controller

The 10 bit wide ATWD output data stream generated during a readout is handled by the Waveform Capture Controller which is also responsible for the waveform buffer management and the trigger packet generation.

Trigger packet generation

Each trigger event generates a trigger packet which is transmitted to the surface. Since the transmission is automatically handled by the Communication Controller as soon as eight bytes are written into the Trigger FIFO, the Waveform Capture Controller's role in trigger packet generation is the assembly of a trigger packet in the FIFO. The format is as follows:

Coarse Time Stamp - 4 Bytes
Event Type - 1 Byte
Empty field - 1 Byte
Event Energy - 2 Bytes

The coarse time stamp is the value of the 32 bit timestamp counter at the time of the trigger signal and can be written immediately after the trigger is sensed. The event type field requires information that is available only after the full ATWD readout is finished, while the event energy is not available before the ATWD and the slow ADC readout is finished.

Waveform Table Organization

The buffer is organized in two parts: the pointer table and the waveform table. The pointer table is 512K bytes deep. Each entry consists of a coarse time stamp for an event (32 bits), an event type field (8 bits) and a pointer to the base address of the waveform data in the waveform table (24 bits). The time stamp and the event type field are identical to the entries in the trigger packet. Altogether 65563 pointers can be stored in the pointer table. They are accessed in a sequential order by the Current Pointer Register, which has

16 active bits and an 8 bit wrap-around extension for control purposes. As soon as the waveform is written and the pointer table is updated, the Current Pointer Register is incremented. The waveform table holds entries of different sizes, depending on the event type. Common to all waveform entries is the first four bytes which describe the event type (for a detailed description see the following table). Most events will consist of a single low resolution readout of channel 0 (128 bytes) followed by slow ADC data (up to 320 bytes). If the Channel 0 Digital Threshold is exceeded by the signal, a high resolution readout or even readout of channel 1 can occur, thereby increasing the size of the entry.

Table 3: Waveform Table entries (to be defined)

Waveform signal processing

The Waveform Capture Controller has to translate the Gray code generated by the ATWD into binary code to allow simple online calculations.

The 128 ATWD samples have a spatial noise of about 25 LSBs (each sample is read out by a different buffer amplifier and comparator, both of which introduce a random offset voltage). In order to subtract the spatial noise, a table with 128 values has to be programed by the CPU with compensation coefficients. After subtraction of the spatial noise coefficients, the samples are compared to the values in the `Ch x Digital_Threshold` registers. Each of these 8bit register values is weighted by a factor of 4 to generate a 10 bit value for the comparison. The result together with the according `Ch x Digitization Flag` is used to determine whether a readout isto be finished or aborted.

Samples are written into a Dual Port Memory and can be formated either as raw (i.e. Gray code) or binary data, depending on the state of the `Raw/Binary_Flag` in the `Readout Control Register`. After a single channel readout is completely finished, the data is written into the waveform buffer memory. Any sample of a low resolution readout with eight or less bits is written into a single byte, nine and ten bit data is written in a compressed format, where 10 bits are aligned in a series of 8 bit words (in case of 9 bits the highest bit is set to 0).

In parallel with the ATWD readout, the Waveform Capture Controller reads in up to 256 samples from the 10 bit slow ADC. The total amount of samples is controlled by the `Slow_ADC_Samples_Register`. Samples are written into the waveform buffer memory as the last data block in 10 bit bit alligned format, therefore up to 320 bytes are needed to store the data. Readout is completed as soon as the complete slow ADC data is written into waveform memory.